DOCKET NO. 8229-017-27 CIP			
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE			
IN RE APPLICATION OF:	JAMES A. HUNTER, ET AL.	ART UNIT:	2872
SERIAL NO.: 10/029,875		EXAMINER:	AMARI, A.
FILING DATE: DECEMBER 31, 2001			
FOR:	HIGH CONTRAST GRATING LIGHT VALVE		

DECLARATION OF JAMES A. HUNTER

ASSISTANT COMMISSIONER FOR PATENTS
PO BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

I, James A. Hunter, do hereby declare and state that:

1. I am a co-inventor of the subject matter claimed in the above-captioned patent application.
2. It is my understanding that one claim of the above-captioned patent application is directed to a reflective light processing element, which may be a grating light valve.
3. I further understand that the grating light valve of the invention includes, as separate elements, a substrate, a dielectric layer formed on the substrate, a conductive trace formed on the dielectric layer and a plurality of ribbons formed above the substrate and the conductive trace. The conductive trace allows charges trapped in the dielectric layer to escape.
4. I am informed that there is no specific purpose recited for this grating light valve, no

specific function, but it is my general understanding, and was prior to December 1989, that a grating light valve is shown to work for its intended purpose when it is demonstrated that it can alter reflective light by movement from conditions of constructive to destructive interference. Specially, a grating light valve, or other light processing element, is shown to work when it modulates the amount of light reflected.

5. Submitted herewith as Exhibit A is a document that was employed at Silicon Light Machines prior to December 1989, referred to as a "runsheet." A runsheet identifies all processes that an actual product is subjected to. The runsheet that is Exhibit A is a runsheet for the preparation of the reflective light processing element having the features described above for the claimed invention of the above-captioned patent application. Exhibit B hereto is a spreadsheet prepared by me, that identifies the correlation between specific steps of the runsheet and a feature of the subject matter referred to above. Claim 1 also corresponds to Claim 1 of the above-captioned patent application.

6. The runsheet that is Exhibit A corresponds to the actual preparation of a prototype of the invention of Claim 1. As it was not a commercial run, nor prepared for a customer, many of the specific details, such as lot number and the like, were not incorporated. As set forth in Exhibit B, certain steps of the run sheet correspond to specific elements or recitations of Claim 1. Each of these is discussed below.

7. Thus, in steps 1 and 2, the runsheet begins with a silicon wafer, which corresponds to the "substrate" of Claim 1. In Step 2 a dry oxidation proceeds on the wafer, which forms an insulating dielectric (silicon dioxide) which corresponds to the recitation of Claim 1 that there be a "dielectric layer formed on the substrate."

8. In step 8 there is reference to deposition of ribbon material, followed in step 9 by the

patterning (ribbon mask) to form "a plurality of ribbons" as required in Claim 1, which is specifically recited in step 11, a step described as the ribbon etch. Thus, an 850 angstroms silicon nitride and 500 angstroms silicon dioxide etch is performed, resulted in a plurality of ribbons, as indicated on the runsheet.

9. At runsheet step 17, the step referred to as a partial release, exposes the dielectric on the substrate without releasing the ribbons fully. This is for the purpose of forming a conductive trace on the dielectric layer. The contact mask of step 18 is a mask for forming the contact for a conductive trace on the dielectric layer.

10. Step 20 of the runsheet is a contact etch step, that is, etching a contact hole for the conductive metal trace formed on the dielectric layer which is formed in Step 21 of the runsheet, metal evaporation. Thereafter, the device comprises the substrate formed at the beginning, step 1, with a dielectric layer thereon, step 2. There is a plurality of ribbons with material deposited, masked and etched in steps 8, 9, and 11 with a conductive trace and contact for the conductive trace formed in steps 17, 18, 20, 21 and 22. Step 23 is a "final release" which releases the ribbons so as to permit movement from constructive to destructive interference conditions.

11. As can be seen, accordingly, by performing the process set forth in the runsheet as was done at Silicon Light Machines by me and individuals working with me and under my direction, the subject matter of Claim 1 can be produced and was produced at Silicon Light Machines prior to December 1989. Moreover, as tested to the satisfaction of myself and my co-inventors, these grating light valves were shown to modulate the amount of light reflected by them from a light source, thereby demonstrating that the grating light values made prior to August 11, 1989, by myself and co-inventors, in fact "worked for the intended purpose" in that they showed utility

as grating light valves.

All statements made herein are of my own knowledge are true and all statements made on information and belief are believed true. Further, I am aware that willful false statements and the like are punishable by fine, imprisonment, or both, 18 USC 1001, and that such willful false statements may jeopardize the validity of U.S. Patent Application 10/029,875 and any patent to issue thereon.

Date 7/4/05

James A. Hunter

EXHIBIT A

_____ *Runsheet* **Lot Number:**

STEP #	STEP	PROCESS	INIT	DATE
1	WAFER START	START P+ SUBSTRATES Prime ___-type <____> Silicon Vendor _____ Resistivity: _____ ohm-cm; Lot #: _____	____	____
2	DRY OXIDATION	Scribe wafers Scribe ID: Lot ID ? ←	____	____
		Post Scribe Clean *(wbnonmetal)* 10 minutes Piranha	____	____
		Pre Diffusion Clean *(wbdiff)* 10 minutes Piranha 30 seconds 50:1 HF 10 minutes $HCL/H_2O_2/H_2O$	____	____
		950° C Dry Oxidation - Target 500 Å *(Tylan 1,3,4)* Recipe: DRY950 Oxidation time: _____ minutes Furnace: tylan _____	____	____ ←
		Measure: Flat Center Top Door: _____ _____ _____ Å Jungle: _____ _____ _____ Å	____	____

STEP #	STEP	PROCESS	INIT	DATE
3	AMORPHOUS SILICON DEP	Pre Clean *(wbmetal)* 6 cycle dump rinse Add 3 1000 Å oxide test wafers source? 550° C amorphous silicon deposition Target 8700Å ? redo ? Recipe: _____ Furnace: TYSTAR1 Deposition rate from test run: _____ Å/min Deposition time: _____ minutes Measure (thickness): Flat Center Top Door: _____ _____ _____ Å Center: _____ _____ _____ Å Jungle: _____ _____ _____ Å	____ ____ ____ ____ ____	____ ____ ____ ____ ____
4	POST MASK	_____ Mask: Level _____ Rev _____ Singe *(singe oven)* 20 minutes 150° C ? Spin Resist *(svgcoat)* Prime, Spin and Prebake Program 1 (run Program 10 to prime lines)	____ ____ ____	____ ____ ____

STEP #	STEP	PROCESS	INIT	DATE
		Expose *(ultratech)* Reticle = _____, Field = _____ Exposure: _____ Focus Offset: _____ Develop/Inspect *(svgdev)* Develop and Postbake Program 1 Wafer #: _____ Verniers: _____ Dagger: _____ Lines: _____ Corners: _____	____ ____	____ ____
5	DESCUM	Descum *(drytek2)* Recipe: descum 2.5 minute etch	____	____
6	POST ETCH	Etch _____ *(drytek2)* Recipe: _____ Etch Time: _____ minutes	____	____

STEP #	STEP	PROCESS	INIT	DATE
		Final Inspect (same wafer from photo): Wafer #: _____ Verniers: _____ Dagger: _____ Lines: _____ Corners: _____	____	____
7	PIRANHA RESIST STRIP	Strip Resist (wet) *(wbnonmetal)* 20 minutes Piranha 10 minutes Piranha	____	____
8	STRATA-GLASS THERMAL NITRIDE DEPOSITION	Outside Services: Strataglass Call courier for pickup (Add 2-3 pre-stress test wafers) LPCVD Nitride: Target 850 Å DCS:NH_3 Ratio: _____ Measure (RI): Flat Center Top Door: _____ _____ _____ Å Center: _____ _____ _____ Å Jungle: _____ _____ _____ Å	← ____ ____ ____	 ____ ____ ____

why?

STEP #	STEP	PROCESS	INIT	DATE
		Measure (thickness): Flat Center Top Door: _____ _____ _____ Å Center: _____ _____ _____ Å Jungle: _____ _____ _____ Å Measure (stress): Door: _____ MPa Center: _____ MPa Jungle: _____ MPa	____	____
9	RIBBON MASK	_____ Mask: Level _____ Rev _____ Singe *(singe oven)* 20 minutes 150° C Spin Resist *(svgcoat)* Prime, Spin and Prebake Program 1 (run Program 10 to prime lines) Expose *(ultratech)* Reticle = _____, Field = _____	____ ____ ____ ____	____ ____ ____ ____

STEP #	STEP	PROCESS	INIT	DATE
		Exposure: _____ Focus Offset: _____ Develop/Inspect *(svgdev)* Develop and Postbake Program 1 Wafer #: _____ Verniers: _____ Dagger: _____ Lines: _____ Corners: _____	____	____
10	DESCUM	Descum *(drytek2)* Recipe: descum 2.5 minute etch	____	____
11	RIBBON ETCH	Etch _____ *(amtetcher)* Recipe: _____ Etch Time: _____ minutes etch 850Å Si3N4 and 500Å SiO2 Resist strip?	____	____

STEP #	STEP	PROCESS	INIT	DATE
		Final Inspect (same wafer from photo): Wafer #: _____ Verniers: _____ Dagger: _____ Lines: _____ Corners: _____	____	____
12	CIS METAL SPUTTER	Pre Clean *(wbmetal)* 30 seconds 50:1 HF Metal Dep (gryphon) _____ Equivalent oxide etch _____ Sputter Deposition Target: 3000Å Measure (Rs): Flat Center Top _____ _____ _____ ohm/sq	____ ____ ____	____ ____ ____
13	M2 MASK	_____ Mask: Level _____ Rev _____ Singe *(singe oven)* 20 minutes 150° C	____ ____	____ ____

STEP #	STEP	PROCESS	INIT	DATE
		Spin Resist *(svgcoat)* Prime, Spin and Prebake Program 1 (run Program 10 to prime lines) Expose *(ultratech)* Reticle = _____, Field = _____ Exposure: _____ Focus Offset: _____ Develop/Inspect *(svgdev)* Develop and Postbake Program 1 Wafer #: _____ Verniers: _____ Dagger: _____ Lines: _____ Corners: _____	____ ____ ____	____ ____ ____
14	DESCUM	Descum *(drytek2)* Recipe: descum 2.5 minute etch	____	____
15	WET METAL ETCH	Pour fresh etchant Etchant: _____ *(wbmetal)*	____	____

STEP #	STEP	PROCESS	INIT	DATE
		Etch metal to clear Etch Time: _____ minutes	____	____
16	RESIST ASH	Strip Resist (dry) *(matrix)* Recipe: newlotemp Strip Time: _____ minutes Post Clean 6 cycle Dump Rinse *(wbmetal)*	____	____
17	PARTIAL RELEASE	WAFERS NEED TO GO TO SLM ← NOE? clean?		
18	CONTACT MASK	_____ Mask: Level _____ Rev _____ Singe *(singe oven)* 20 minutes 150° C Spin Resist *(svgcoat)* Prime, Spin and Prebake Program 1 (run Program 10 to prime lines)	____ ____ ____	____ ____ ____

STEP #	STEP	PROCESS	INIT	DATE
		Expose *(ultratech)* Reticle = _____, Field = _____ Exposure: _____ Focus Offset: _____	____	____
		Develop/Inspect *(svgdev)* Develop and Postbake Program 1 Wafer #: _____ Verniers: _____ Dagger: _____ Lines: _____ Corners: _____	____	____
19	DESCUM	Descum *(drytek2)* Recipe: descum 2.5 minute etch	____	____
20	CONTACT ETCH	Etch _____ *(amtetcher)* Recipe: _____ Etch Time: _____ minutes	____	____

STEP #	STEP	PROCESS	INIT	DATE
		Final Inspect (same wafer from photo): Wafer #: _____ Verniers: _____ Dagger: _____ Lines: _____ Corners: _____	____	____
21	METAL EVAP	WAFERS NEED TO GO TO LANCE GODDARD	500Å	
22	ALLOY	simulate real furnace?		
23	FINAL RELEASE	WAFERS NEED TO GO TO SLM		

EXHIBIT B

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Step #	Step Name	Comments	Claim Reference
1	WAFER START	Starting Si Substrate	Claim 1, "a substrate"
2	DRY OXIDATION	Grow an insulating dielectric	Claim 1, "a dielectric layer formed on the substrate"
3	AMORPHOUS SILICON DEP	Deposit Si sacrifiical layer	NA
4	POST MASK	Photo patterning of ribbon anchor	NA
5	DESCUM	Ashing of residual photoresist	NA
6	POST ETCH	Forms ribbon anchor "mold"	NA
7	PIRANHA RESIST STRIP	Strips resist	NA
8	STRATAGLASS THERMAL NITRIDE DEPOSITION	Ribbon material deposition	Claim 1, "a plurality of ribbons..."
9	RIBBON MASK	Photo patterning of ribbon	Claim 1, "a plurality of ribbons..."
10	DESCUM	Ashing of residual photoresist	NA
11	RIBBON ETCH	Etching of ribbon	Claim 1, "a plurality of ribbons..."
12	CIS METAL SPUTTER	Deposition of thick metal wiring	NA
13	M2 MASK	Photo patterning of thick meta wiring	NA
14	DESCUM	Ashing of residual photoresist	NA
15	WET METAL ETCH	Etching of thick metal wiring	NA
16	RESIST ASH	Strips resist	NA
17	PARTIAL RELEASE	Exposes dielectric on substrate without releasing ribbons fully	Claim 1, "a conductive trace on the dielectric layer.."
18	CONTACT MASK	Photo patterning of contact hole for conductive metal trace	Claim 1, contact for "a conductive trace on the dielectric layer.."
19	DESCUM	Ashing of residual photoresist	NA
20	CONTACT ETCH	Etching of contact hole for conductive metal trace	Claim 1, contact for "a conductive trace on the dielectric layer.."
21	METAL EVAP	Formation of conductive trace	Claim 1, "a conductive trace on the dielectric layer.."
22	ALLOY	Sinters contact	Claim 1, contact for "a conductive trace on the dielectric layer.."
23	FINAL RELEASE	Fully releases ribbons	Claim 1, "a plurality of ribbons..."